AD-A077 340 WOODS HOLE OCEANOGRAPHIC INSTITUTION MASS F/G 14/3
A MEMODYNE 3722 CASSETTE READER SYSTEM FOR THE HP 2100 COMPUTER--ETC(U)
OCT 79 W E TERRY N00014-76-C-0197
UNCLASSIFIED WHOI-79-75 NL

| OF |

AD
A077340

END
DATE
FILMED
1-80
DDC

WHO

ls Hole

LEV

Oceanographi

Instit

D

NOV

A MEMODYNE 3722 CASSETTE R
SYSTEM FOR THE HP 2100 CO
AND PROGRAM CARP

by

W. E. Terry

October 1979

TECHNICAL REPORT

Prepared for the Office of Naval R
under Contract N00014-76-C-0197; N

Approved for public release; distr
unlimited.

UNCLASSIFIED 10/79

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER (14) WHOI-79-75	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) (6) A MEMODYNE 3722 CASSETTE READER SYSTEM FOR THE HP 2100 COMPUTER AND PROGRAM CARP		5. TYPE OF REPORT & PERIOD COVERED (9) Technical rept.
		6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) (10) W. E. Terry (12) 37		8. CONTRACT OR GRANT NUMBER(s) (15) N00014-76-C-0197
9. PERFORMING ORGANIZATION NAME AND ADDRESS Woods Hole Oceanographic Institution Woods Hole, MA 02543		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS NR 083-400
11. CONTROLLING OFFICE NAME AND ADDRESS NORDA National Space Technology Laboratory Bay St. Louis, MS 39529		12. REPORT DATE (11) Oct[redacted]79
		13. NUMBER OF PAGES 24
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office) 381 000		15. SECURITY CLASS. (of this report) Unclassified
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

1. Memodyne 3722 cassette reader
2. Cassette reader
3. CARP

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report describes a special purpose electronic interface between the Memodyne 3722 High Speed Cassette Tape Reader and the Hewlett Packard 2100 series computer with program CARP using an HP 12566 interface. A description of the operation and alignment procedures is included.

WHOI-79-75

A MEMODYNE 3722 CASSETTE READER SYSTEM FOR THE HP 2100 COMPUTER AND PROGRAM CARP

by

W. E. Terry

WOODS HOLE OCEANOGRAPHIC INSTITUTION
Woods Hole, Massachusetts 02543

October 1979

TECHNICAL REPORT

Prepared for the Office of Naval Research under Contract N00014-76-C-0197; NR 083-004.

Approved for Distribution Earl E. Hays
Earl E. Hays, Chairman
Department of Ocean Engineering

TABLE OF CONTENTS

ABSTRACT

This report describes a special purpose electronic interface between the Memodyne 3722 High Speed Cassette Tape Reader and the Hewlett Packard 2100 series computer with program CARP using an HP 12566 interface. A description of the operation and alignment procedures is included.

INTRODUCTION

The use of incremental digital cassette recorders in off-line data storage has increased significantly in the past few years. Several systems, using standard Phillips cassettes with the Complimentary Non-Return to Zero Inverted (CNRZI) format at 615 bits per inch, are manufactured by at least two companies. These systems are small in size, are quite flexible with their input requirements, and can store up to 2×10^6 bits with a 282 ft. tape. Models are available that incorporate CMOS logic to minimize power consumption.

A few of these systems have been recently incorporated in oceanographic instrumentation. A need was seen to be able to read these tapes using data processing techniques currently in use at the Woods Hole Oceanographic Institution (W.H.O.I.), leading to the design of this interface.

The interface described in this report is designed to take the serial data output of the Memodyne Model 3722 High Speed Tape Reader and output parallel data compatible with the program CARP, Vers. 17, developed at W.H.O.I. (Hunt, 1971) using a Hewlett Packard 2100 series computer with the HP 12566 positive true interface (Hewlett Packard, 1972). The outputs of the interface are in the same format as the 850 Current Meter H.P. Interface developed by K. Peal (1973) for use on the W.H.O.I. Buoy Group Computer.

The output of the interface is a sixteen bit parallel word consisting of twelve data bits and four message bits which is transferred when the interface flags the computer. The output is available at J-5 on the backpanel of the modified 3722 reader as shown in Figures 12 and 13. The computer flag is a 20 μsec negative true pulse. Bit 0 is an error bit that indicates when the data in the current record are in error.

The error bit signifies that a multiple of four bits has not been counted during the record. Bits 1 and 2 are used to indicate the number of four bit bytes in the word. The byte count is normally three (bits 1 and 2 high) indicating 12 bits, but will be 0, 1, or 2 with the last word in a record. The data bits are 3 through 14 with the leading bit in the data stream being computer bit 14 for a twelve bit word. The end of cassette record (EOR) is indicated by bit 15.

To avoid confusion, it is important to note that in Memodyne terminology bits are grouped into words usually separated by two bit gaps. Words are grouped into files usually separated by 12 bit gaps. In CARP terminology data words consist of 3 bytes (12 bits). The words are grouped into cassette records separated by an EOR, and the records are grouped into a file.

MEMODYNE 3722 READER

The Memodyne 3722 High Speed Reader is designed for reading standard Phillips cassettes with a CNRZI format. The CNRZI technique is a two track format in which a flux change on Track 1 indicates a "0" and a flux change on Track 2 indicates a "1". This permits recovery of a clock pulse independent of tape speed with each bit. Figure 2 shows an example of the CNRZI format. Further information on this and other recording formats can be found in Cassette Recording for Off-line Storage (Memodyne, a.) and in Reference Data for Radio Engineers (Sams Inc., 1975).

The Model 3722 can be internally adjusted to read tape densities of 300 to 1200 bits per inch (bpi) with 615 bpi being standard. The tape speed is 20 inches per second (ips) which gives a data output rate of 12,300 bits/second at 615 bpi. The rewind speed is 100 ips.

The reader is designed for reading cassette tapes written on Memodyne incremental recorders such as the Model 3243 and the 200 and 500 series. These recorders permit word lengths of 8, 12, or 16 bits. Words are separated by two bit gaps and are grouped into files of up to 64 words. The inter-file gap may be 12 or 16 bits. This format is compatible with other recorders such as the Datel LPS-16 and ICT-WZ series.

An integral part of the Memodyne Model 3722 is the Model 763 high speed digital cassette recorder consisting of the tape transport and a circuit board, J2. The board controls the tape motion and the digital recording and playback. The recording circuitry is not used with the Model 3722. The 763 board is controlled by the Model 922 controller board, J3. Data from the two tape tracks are amplified by the 763 board to TTL levels and then transferred to the 922 board.

A diagram of the essential electronics of the 922 board used for the interface is given in Figure 3. A timing diagram is shown in Figure 2. Data in each channel is inverted and a positive pulse is generated at each detected flux change by an Exclusive OR edge detector. These pulses drive an Exclusive OR gate to produce a clock pulse with each flux change. The monostable multivibrator increases the pulse width to about .8 μsec. These pulses clock the 922 shift registers for the 3722's serial to parallel conversion. The edge pulses from the two channels are also used as inputs to an R-S flipflop to which outputs an inverted data level for the 922 shift registers. The serial data level and the clock are both inverted to provide positive true clock and data levels.

The outputs of the Model 3722 are TTL level. The output format options are 8, 12, or 16 bit parallel, and serial. A clock is available.

OPERATION

Control of the Model 3722 may be achieved by the front panel switches or by external signals at the back panel connector, J-2, when the EXTERNAL switch is depressed. The front panel layout is shown in Figure 1.

The cassette is inserted with the tape edge at the bottom and the takeup reel at the right. After a five to ten second delay, the STATUS LAMP should come on indicating a ready state. The RUN and REWIND commands are ignored when the STATUS lamp is off. An interlock, mating with a groove in the cassette prevents tapes from being read backwards. Tape placed over the groove will permit a tape that has been recorded backwards to be read.

The REWIND switch is lit when the clear leader is detected at the end of the tape. The rewind cycle is started by the STANDBY command followed by the REWIND command. The rewind cycle is terminated at the end of the tape or by a RUN command which starts the read cycle. The REWIND command is ignored during the read cycle.

The read cycle is started by the RUN command. The Model 3722 will read until a three inch end-of-data gap is detected or the end of the tape is reached. Data following this gap may be read by starting another read cycle without rewinding the tape. The read cycle may also be terminated by the STANDBY command. The STANDBY command is ignored during the rewind cycle.

Further information on the Model 3722 can be obtained from the Model 3722 Instruction Manual (Memodyne, b.).

TYPICAL READ SEQUENCE

1. Turn reader power ON. The power switch should light. The EXT (external) switch should be off.
2. Insert cassette into tape drive door with tape edge down. The take up reel is on the right. Close the door.
3. The status light will come on after about five seconds. It will not light if the tape is inserted backwards.
4. Press STANDBY, REWIND.
5. Program CARP should now be made ready at the "COMMENTS?" request. See CARP write up for details.
6. Start cassette by pressing RUN.
7. Tape will be read until a three inch gap or end of the tape is reached. To continue reading after the three inch gap, press RUN. To stop the read cycle press STANDBY.
8. Rewind the tape by pressing STANDBY, REWIND.

Detailed instructions can be found in the Operation section of this manual, write up for CARP, and the Memodyne Model 3722 Instruction Manual.

INTERFACE CIRCUIT DESCRIPTION

The interface schematic is shown in Figure 4. A timing diagram is shown in Figure 5. The circuit board layout is in Figure 6. Integrated circuit pin numbers are referred to as U# - (pin #). The card edge connections are referred to as pin #. The interface card plugs into connector J4 in the 3722 reader card cage. Other pin numbers not on J4 are referred to as pin # (J#). Interconnection lists are given in Figures 8, 9, 10, 11,

12, and 13. Power is obtained from the 3722 +5 V supply. All grounds are connected to a common point to avoid ground loops.

All integrated circuits used in the interface are low power Schottky TTL. Levels greater than +2.4 V are logic "1" and levels less than +.8 V are logic "0". A 10 μF, 25 volt capacitor is present at the power supply input, and a .015 μF capacitor is at each IC package input for despiking purposes.

In Figure 4 the clock pulses at pin C load and shift the data through the shift registers, U1 and U2. In addition, the counter, U4, is clocked, and the EOR one-shot (U3B) is retriggered by the pulses. U6A-3 indicates a count of twelve bits by going low and through U6B-6 sets the negative true computer flag U7A-4. The flag is a 20 μsec pulse controlled by R_{13}. The trailing edge of the flag pulse triggers a 5 μsec clear pulse at U3A-4 and U3A-13, clearing the shift registers and the counter. The clear pulse width is controlled by R_{11}.

The end of record gap is detected by an absence of clock pulses at U3B-10. This retriggerable one-shot is adjusted by R_9 for a delay of 6 bits. The two bit gaps between words are ignored. When the 6 bit gap is detected, the computer flag (pin K) is set, and the EOR bit goes high. If a multiple of four bits has not been counted at the EOR, U5D pin 13 sets the error bit U5C-10 (pin R) indicating that an <u>error has occurred during the record</u>. The timing diagram, Figure 5, gives an example of the case where only eleven bits have been detected at the end of a record.

With each 16 bit parallel computer input word, the Byte Count bits, pins N and M, indicate the number of four bit characters or bytes. This is normally three, although at the end of a record this will be 0, 1, or 2. This allows tape formats with words in multiples of four bits

to be read.

A list of the interface outputs to the computer is given in Figure 13.

Signals available at the front panel BNC's are:

Serial Data	Pin A
$\overline{\text{Clear}}$	Pin B
Serial Clock	Pin C
End of record	Pin F
Flag (neg. true)	Pin K
ERROR	Pin R
Channel 1	Pin 1 (J-3)
Channel 2	Pin 2 (J-3)

INTERFACE ALIGNMENT AND TESTING PROCEDURE

A quick check of operating parameters can be made by observing the signals available at the front panel BNC connectors using a known test tape. A multichannel oscilloscope is necessary. A counter with "width B" or "time A to B" and "events A during B" modes, while not necessary, is useful.

Using the oscilloscope the serial clock, the flag and the EOR can be observed using the rising EOR edge as a trigger. Reference should be made to the timing diagram in Figure 5. EOR should go high after a six bit delay at the end of the record. This delay is adjusted with R_9 (Figure 6). The flag pulse should occur after each twelve bit word and also with the EOR leading edge.

Due to normal fluctuations in the data rate, the flag pulse width is best adjusted with a counter in the "width B" mode. The flag is negative true, i.e., the leading edge is the falling edge. The pulse width should be 20 μsec and is adjusted with R_{13}.

The clear pulse may also be adjusted with the counter in the same manner. The BNC output is negative true. The clear pulse may be viewed using the leading (falling) edge of the flag pulse as a trigger. The clear pulse should be 5 μsec, and is adjusted with R_{11}.

Using the counter in the "events A during B" mode, one can count the number of clock pulses per word (or per record). The rising edge of the flag pulse (or the EOR pulse) is used as a trigger.

If a counter is not available, timing adjustments are simplified by using known input signals. The board must be removed from the 3722 card cage. The cage must be removed by removing four cage screws inside the bottom cover of the 3722 chassis. The cage is lifted out of the top of the 3722. Notice that wiring is connected to both the front and back of the card cage.

With the interface card removed, connections should be made as follows: 5 V is applied to pin 1 and GND to pin Z. Pin A (DATA) should be tied to pin 1 or Z as described below.

A digital pulse generator may be used to supply a counted or gated burst of 12.3 KHz pulses to the clock input (pin C). This allows forcing of the error detection by looking at groups of 11, 12, and 13 bits. The error flag should be present at the end of record when bursts which are not multiples of four are present. The burst repetition rate should be less than about 400 Hz to allow the EOR detector to remain untriggered when looking at bursts of up to 24 bits. The steady clock at pin C

allows the flag and clear pulses to be seen without jitter and adjusted as described above.

The shift registers may be checked by observing their output as the Serial Data line (pin A) is tied high or low. The registers are clocked on the trailing edge of the clock pulses and cleared by the leading edge (falling edge) of the clear pulses at U3-4.

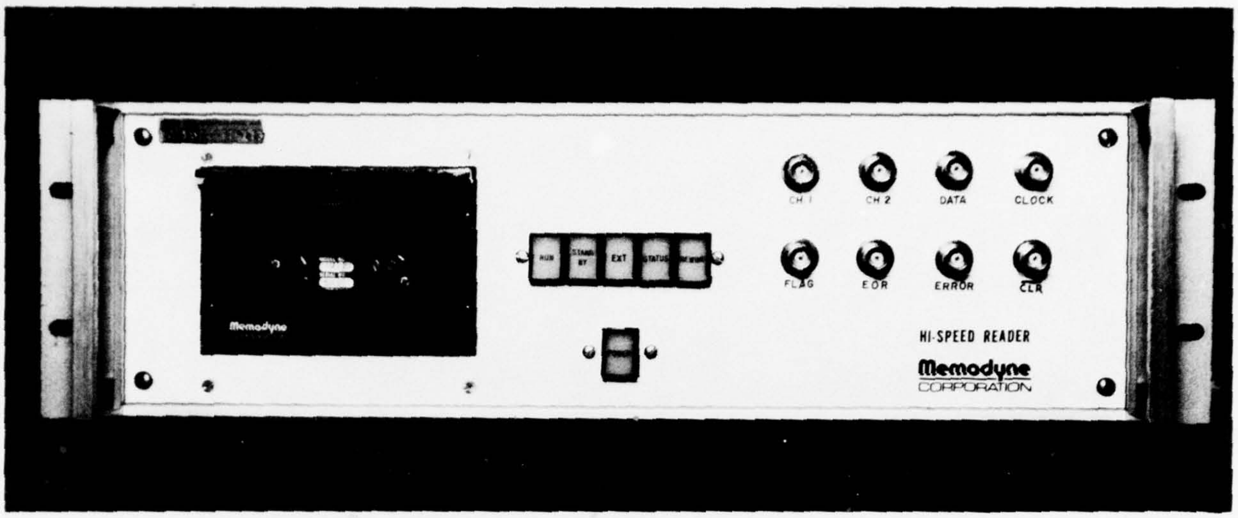

Figure 1a. Memodyne 3722 with modified front panel

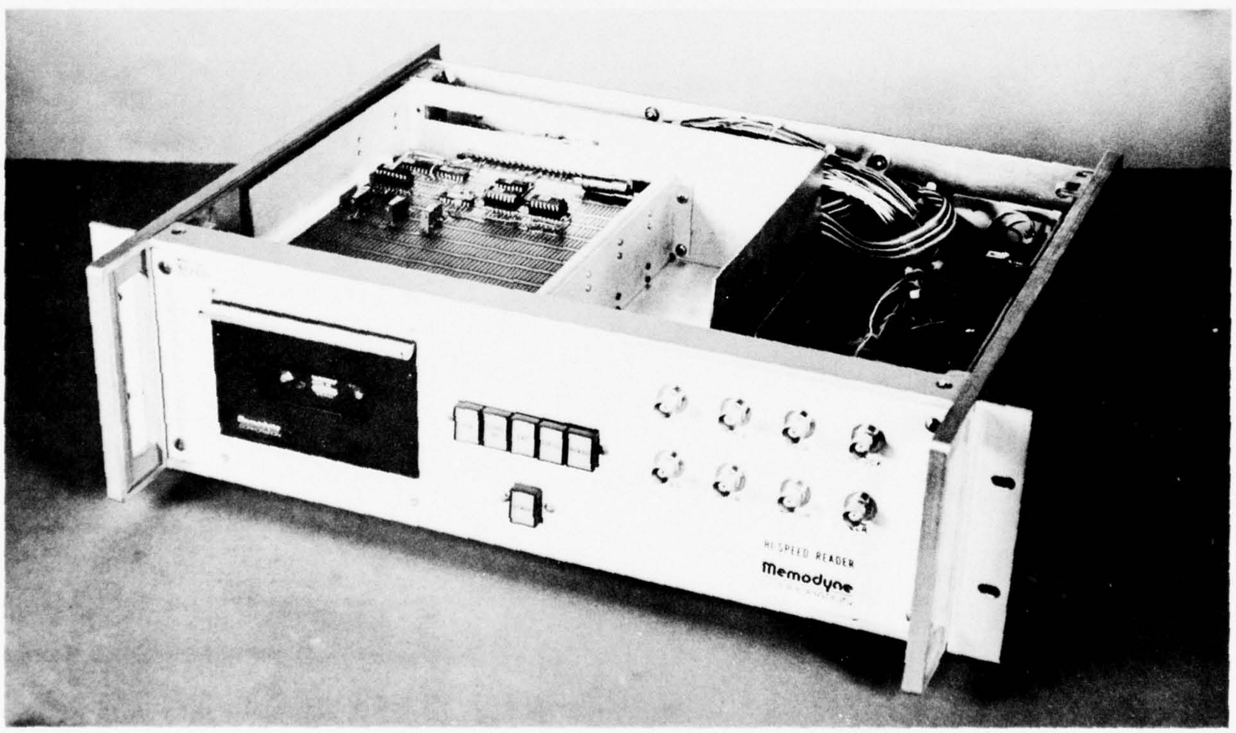

Figure 1b. Modified Reader with interface board shown

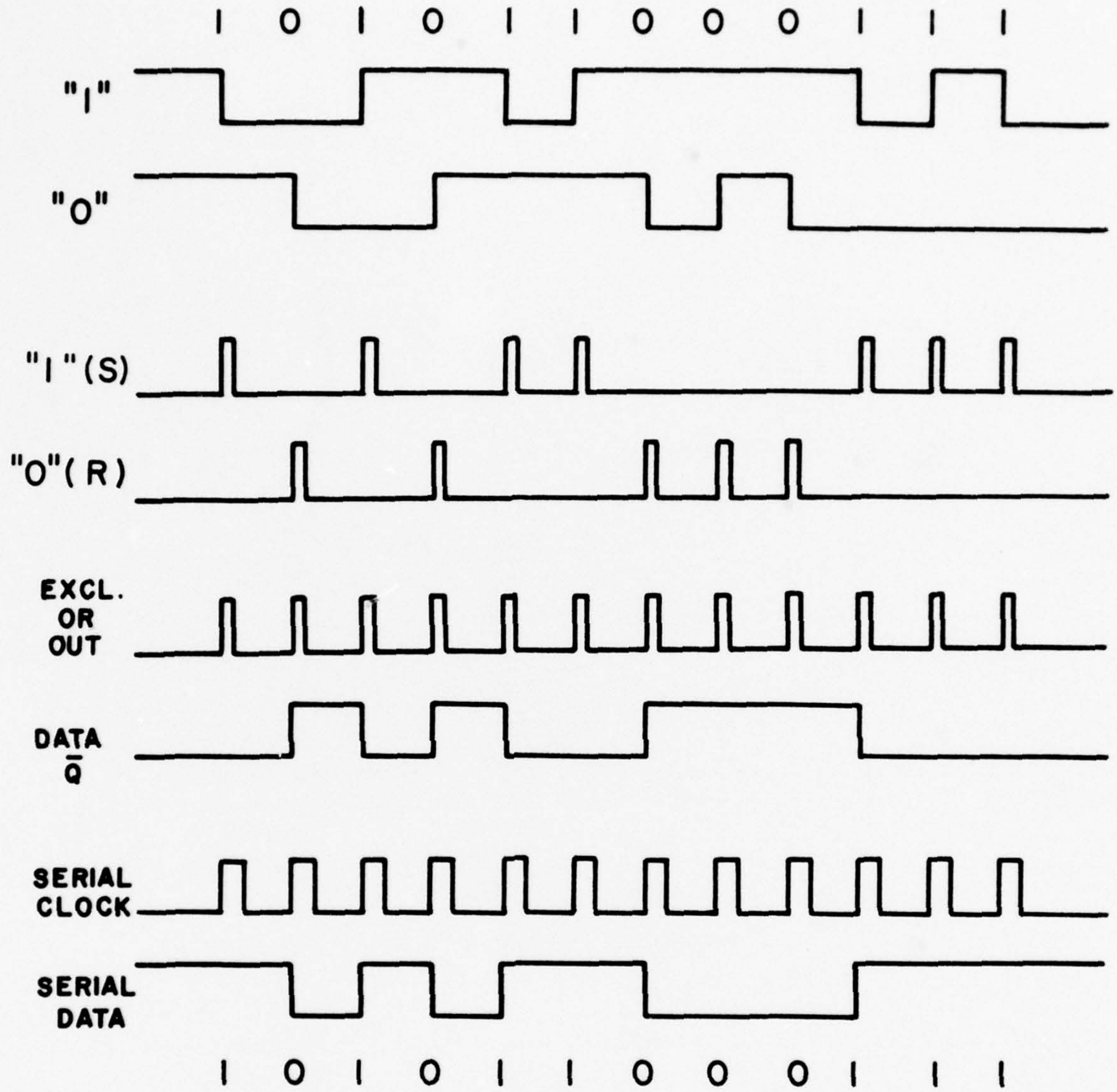

Figure 2. CNRZI Format and timing diagram for Figure 3

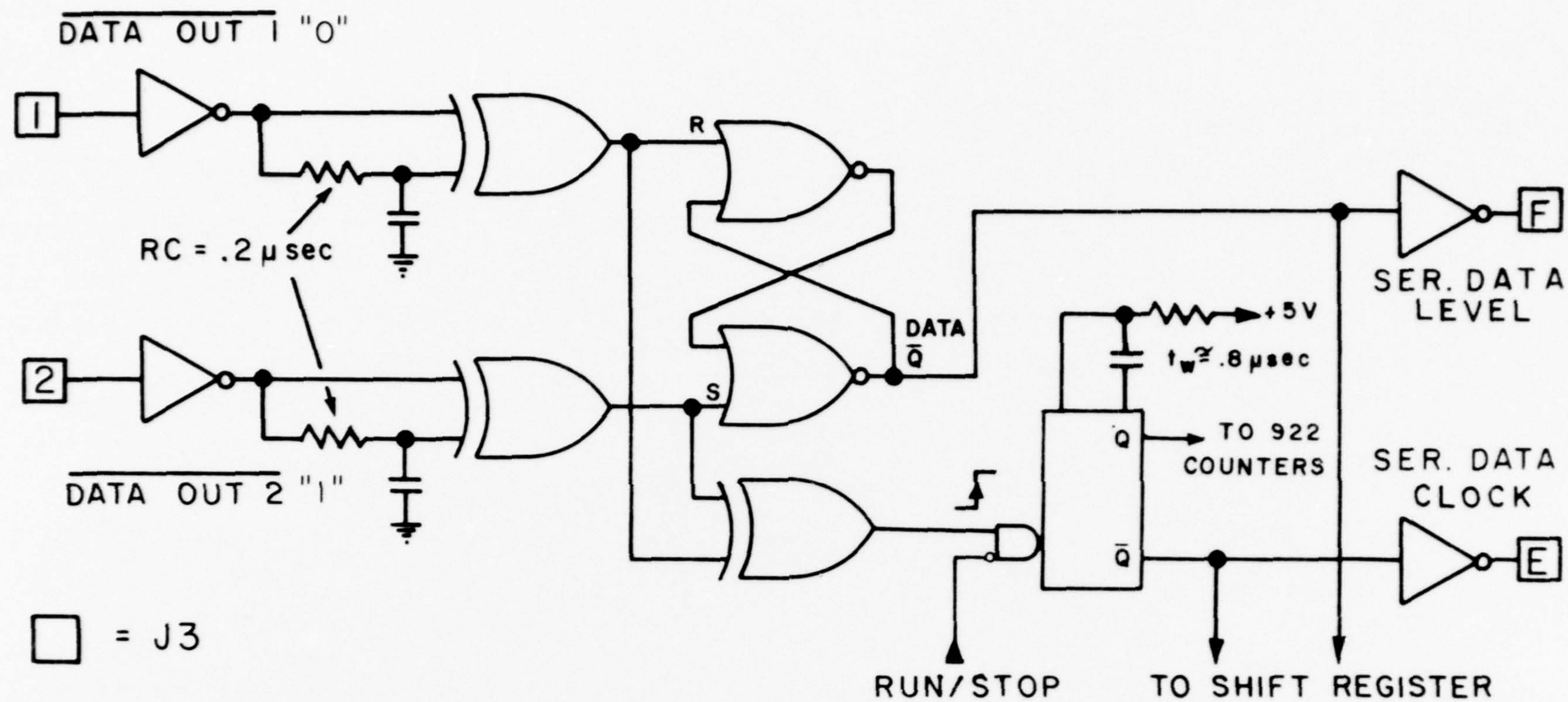

Figure 3. Essential Electronics for decoding CNRZI format to a serial data stream

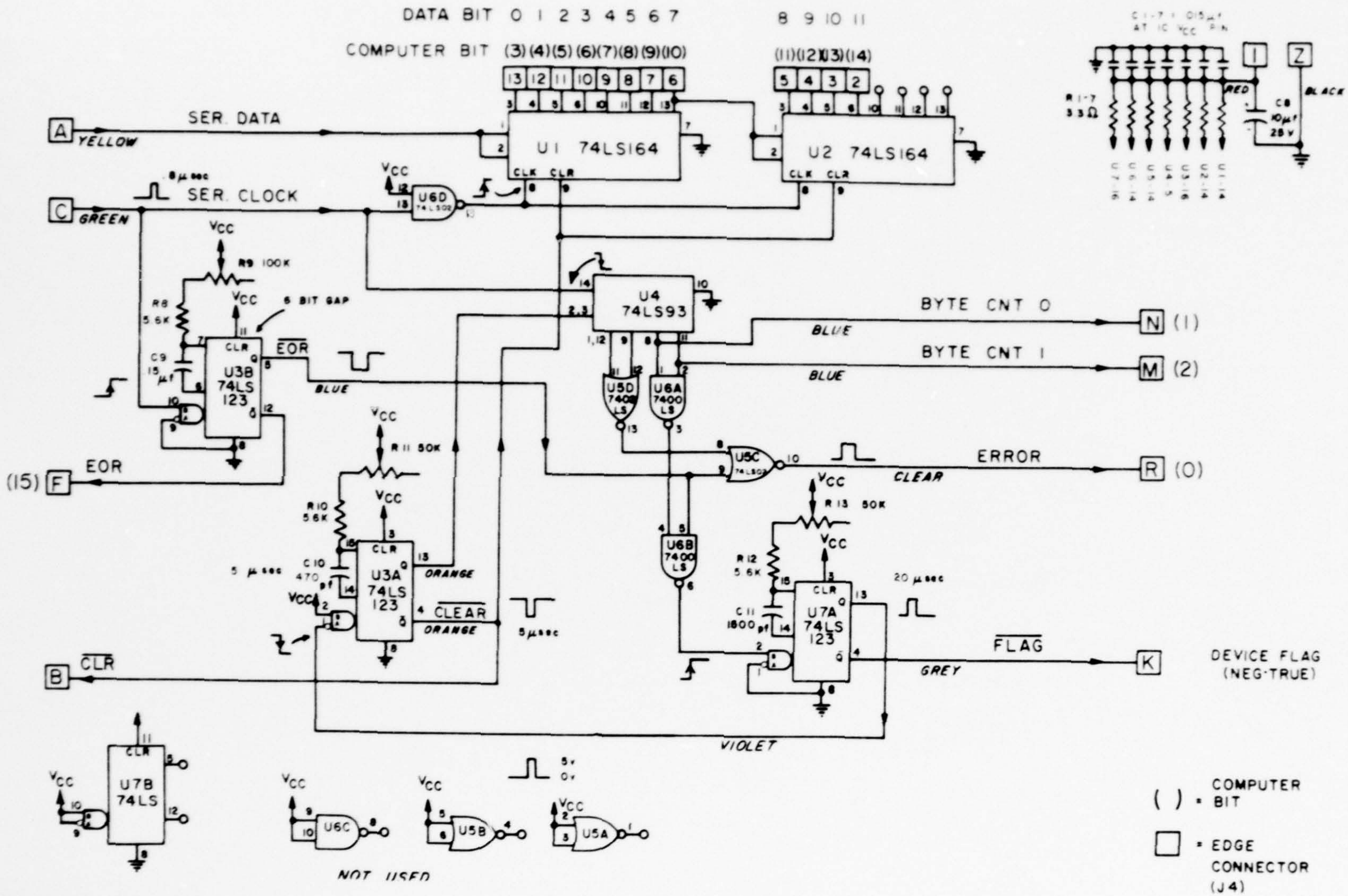

Figure 4. Interface Schematic

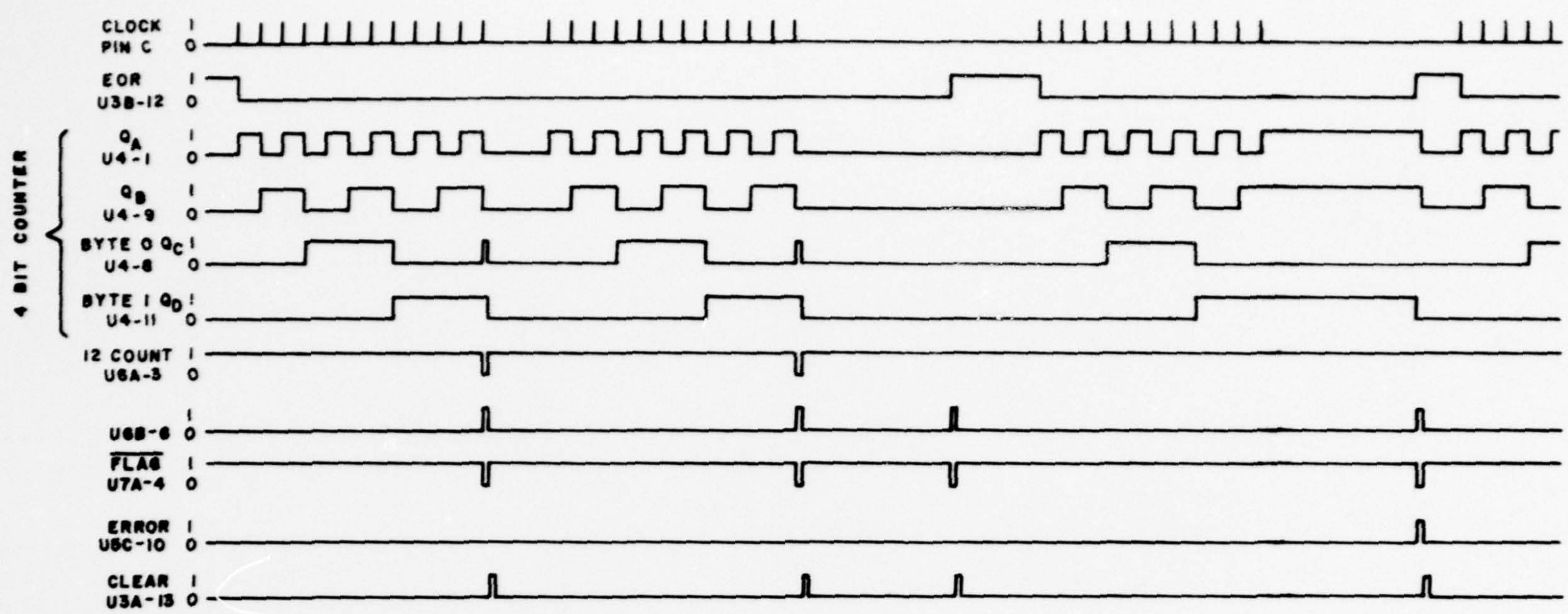

Figure 5. Interface Timing Diagram

The clock pulses show a 24 bit record followed by a 10 bit gap, and an error record followed by an 8 bit gap (CARP terminology). The 2 bit interword gap can be seen at the end of the first 12 bits. The EOR line triggers on the leading edge of the first new clock pulse at the start of a new record. After a 488 μsec (6 bit gap), the EOR line goes high until it is reset with new clock pulses.

The counter (U4) clocks on the falling edge of the clock. The outputs of the counter, Q_A, Q_B, Q_C (Byte 0), and Q_D (Byte 1) count to a count of 12 (U6-3) and set the computer flag through U6-6. The rising EOR edge also sets the flag through U6-6. $\overline{\text{Flag}}$ is shown as the computer uses a negative true flag.

The trailing edge of the 20 μsec flag pulse triggers a 5 μsec clear pulse which clears the counter and the shift registers.

The 11 bit error record shows Q_A and Q_B high at EOR. This is not a multiple of 4, thus the error bit (U5-10) is set with $\overline{\text{Flag}}$ at EOR. Byte count 1 is high indicating two characters (8 bits) in the last word. The error bit indicates the bit count is not a multiple of four for the record, not necessarily the last word in the record.

The last word shows the case where an 8 bit EOR gap exists. Because the gap one-shot retriggers on the leading (rising) edge of the clock pulses, the EOR gap length is not critical.

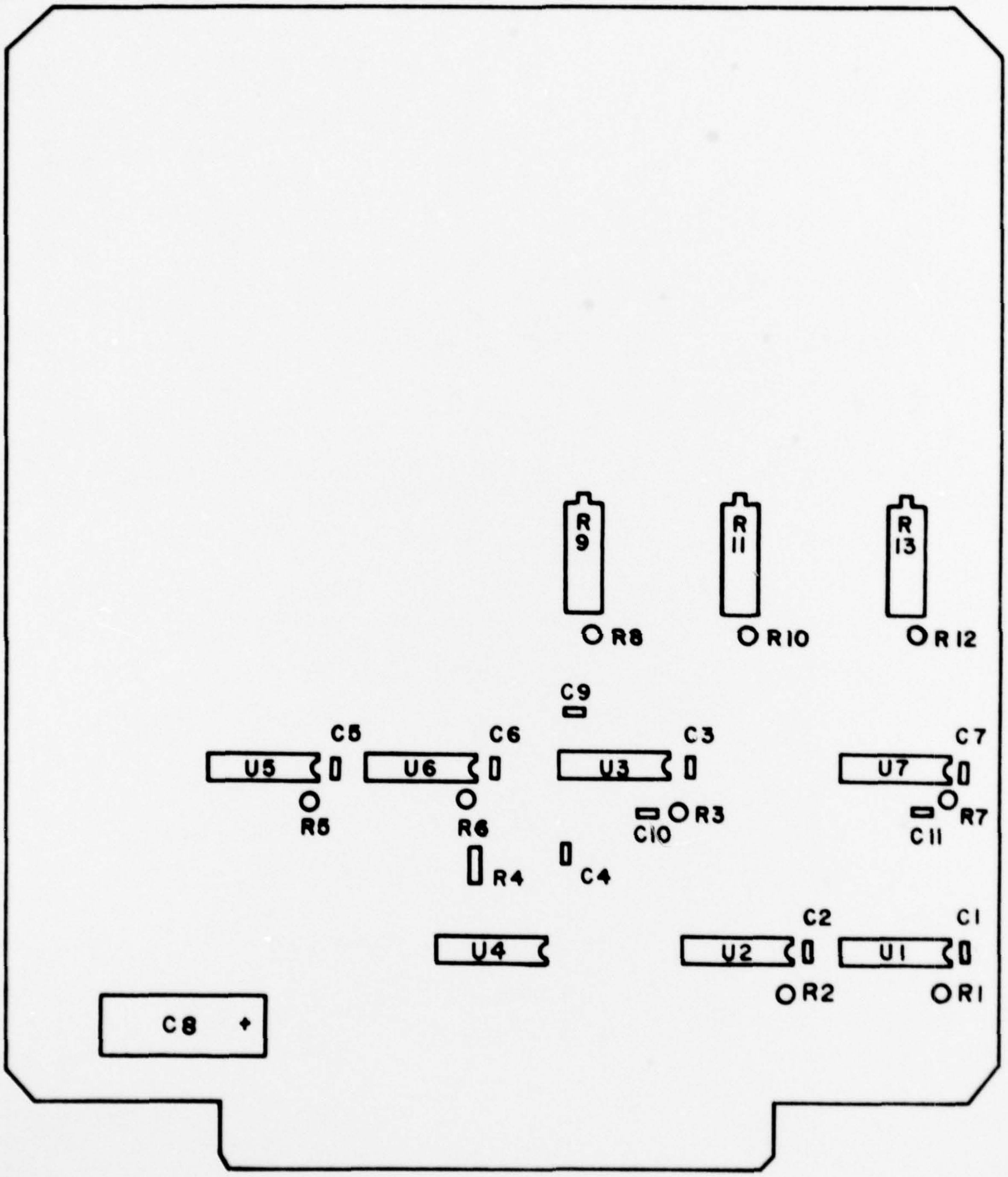

Figure 6. Component Placement

PARTS LIST

Circuit Board	12-DE5-GP	Douglass Electronics
BNC Jacks	3778	Pamona
C_1 - C_7	.015 μf	
C_8	10 μf, 25 V, electrolytic	
C9	.15 μf	
C_{10}	470 pf	
C_{11}	1500 pf	
J_4	50-44A-30	Cinch
J_5	DC 37S	Cannon
U_1, U_2	74LS164	
U_3	74LS123	
U_4	74LS93	
U_5	74LS02	
U_6	74LS00	
U_7	74LS123	
R_1 - R_7	3.3 Ω, ¼ W, 5%	
R_8	5.6 KΩ, ¼ W, 5%	
R_9	100 KΩ Trimpot	
R_{10}	5.6 KΩ, ¼ W, 5%	
R_{11}	50 KΩ Trimpot	
R_{12}	5.6 KΩ, ¼ W, 5%	
R_{13}	50 KΩ Trimpot	

Figure 7

J1 - MEMODYNE 763 BOARD

PIN NO.	FUNCTION	SOURCE	CONNECTS WITH	COLOR
B1	DIG. GND		GND	BLK
B2	+5 V		+5 V	ORG
B3	- FWD/REV		J3-8	WHT/ORG
B4	FAST/-SLOW		J3-7	WHT/RED
B5	- RUN/STOP		J3-6	WHT/BRN
B6	- DATA IN 1		GND	BLK
B7	WRITE/-READ		GND	BLK
B8	- DATA IN 2		GND	BLK
B9				
B10				
B11	- DATA OUT 1	X	J3-1	BRN
B12	BEOT OUT	X	J3-5	WHT/BLK
B13	FILE PROTECT			
B14	- BUSY/READY	X	J3-3	GRY
B15	- DATA OUT 2	X	J3-2	BLU
B16	- CIP	X	J3-4	WHT
B17				
B18	+15 V		+15 V	RED
B19				
B20	GND		GND	BLK
B21				
B22				
B23				
B24				
B25				
B26				
B27				
B28				
B29				
B30				
B31				
B32				
B33				
B34	GND		GND	BLK
B35				
B36	+15 V		+15 V	RED
B37				
B38	GND		GND	BLK
B39				
B40	-15 V		-15 V	VIO

Figure 8

J2 - MEMODYNE BACK PANEL

PIN NO.	FUNCTION	SOURCE	CONNECTS WITH	COLOR
1	2^0		J3-Z	BRN
2	2^1		J3-Y	VIO/WHT
3	2^2		J3-X	BLU/WHT
4	2^3		J3-W	GRN/WHT
5	2^4		J3-V	YEL/WHT
6	2^5		J3-U	RED/BLK
7	2^6		J3-T	BRN/WHT
8	2^7		J3-S	BLK/WHT
9	2^8		J3-R	WHT/GRY
10	2^9		J3-P	WHT/VIO
11	2^{10}		J3-N	WHT/BLU
12	2^{11}		J3-M	WHT/GRN
13	2^{12}		J3-L	WHT/YEL
14	2^{13}		J3-K	WHT/RED
15	2^{14}		J3-J	WHT/BRN
16	2^{15}		J3-H	WHT/BLK
17	- WORD SYNC		J3-A	BRN
18	EOF		J3-B	YEL
19	- EXT. STOP		J3-19	GRY
20	BUSY/-READY		J3-D	BLU
21	- CIP		J3-9	YEL
22	- EOT/BOT		J3-10	GRN
23	- END OF DATA		J3-C	GRN
24	GND		GND	BLK
25	GND		GND	BLK
26	SER. DATA		J3-F	WHT
27	SER. CLOCK		J3-E	GRY
28	- EXT REWIND		J3-18	BLU
29				
30				
31				
32				
33				
34				
35	- EXT START		J3-20	WHT
36				

Figure 9

J3 - MEMODYNE 922 CONTROLLER BOARD

PIN NO.	FUNCTION	SOURCE	CONNECTS WITH	COLOR
1	- DATA OUT 1		J1 - B11 BNC	BRN
2	- DATA OUT 2		J1 - B15 BNC	BLU
3	- BUSY/READY		J1 - B14	GRY
4	- CIP		J1 - B16	WHT
5	BEOT OUT		J1 - B12	WHT/BLK
6	- RUN/STOP	X	J1 - B5	WHT/BRN
7	FAST/-SLOW	X	J1 - B4	WHT/RED
8	- FWD/REV	X	J1 - B3	WHT/ORG
9	- CIP	X	J2 - 21	YEL
10	- EOT + BOT	X	J2 - 22	GRN
11	+5 V		+5 V	ORG
12	GND		GND	BLK
13	STAT. LMP. DR.	X	S5 - 2 COM	WHT/YEL
14	BOT/EOT LMP.	X	S6 - 2 COM	WHT/GRN
15	- RWD SWITCH		S6 - 3 NO	WHT/BLU
16	- STOP SWITCH		S2 - 3 NC	WHT/VIO
17	- START SWITCH		S2 - 3 NO	WHT/GRY
18	- EXT. RWD.		J2 - 28	BLU
19	- EXT. STOP		J2 - 19	GRY
20	- EXT. START		J2 - 35	WHT
21	EXT. SWITCH		S4 - 3 NC	BLK/WHT
22	- EXT. SWITCH		S4 - 3 NO	BRN/WHT
A	- WORD SYNC	X	J2 - 17	BRN
B	E.O. FILE	X	J2 - 18	YEL
C	- E.O. DATA	X	J2 - 23	GRN
D	BUSY/-READY	X	J2 - 20	BLU
E	SER. CLOCK	X	J2 - 27 BNC	GRY
F	SER. DATA	X	J2 - 26 BNC	WHT
H	2^{15}	X	J2 - 16	WHT/BLK
J	2^{14}	X	J2 - 15	WHT/BRN
K	2^{13}	X	J2 - 14	WHT/RED
L	2^{12}	X	J2 - 13	WHT/YEL
M	2^{11}	X	J2 - 12	WHT/GRN
N	2^{10}	X	J2 - 11	WHT/BLU
P	2^{9}	X	J2 - 10	WHT/VIO
R	2^{8}	X	J2 - 9	WHT/GRY
S	2^{7}	X	J2 - 8	BLK/WHT
T	2^{6}	X	J2 - 7	BRN/WHT
U	2^{5}	X	J2 - 6	RED/BLK
V	2^{4}	X	J2 - 5	YEL/WHT
W	2^{3}	X	J2 - 4	GRN/WHT
X	2^{2}	X	J2 - 3	BLU/WHT
Y	2^{1}	X	J2 - 2	VIO/WHT
Z	2^{0}	X	J2 - 1	BRN

Figure 10

BNC = FRONT PANEL BNC

J4 - CARP INTERFACE BOARD

PIN NO.	FUNCTION	SOURCE	CONNECTS WITH	COLOR
1	+5 V		+5 V	ORG
2	DATA BIT 11/COMP BIT 14	X	J5 - 15	YEL R
3	DATA BIT 10/COMP BIT 13	X	J5 - 14	GRN R
4	DATA BIT 9/COMP BIT 12	X	J5 - 13	BLU R
5	DATA BIT 8/COMP BIT 11	X	J5 - 12	VIO R
6	DATA BIT 7/COMP BIT 10	X	J5 - 11	GRY R
7	DATA BIT 6/COMP BIT 9	X	J5 - 10	WHT R
8	DATA BIT 5/COMP BIT 8	X	J5 - 9	BLK R
9	DATA BIT 4/COMP BIT 7	X	J5 - 8	BRN R
10	DATA BIT 3/COMP BIT 6	X	J5 - 7	RED R
11	DATA BIT 2/COMP BIT 5	X	J5 - 6	ORG R
12	DATA BIT 1/COMP BIT 4	X	J5 - 5	YEL R
13	DATA BIT 0/COMP BIT 3	X	J5 - 4	GRN R
14				
15				
16				
17				
18				
19				
20				
21				
22				
A	SER. DATA		J3 - F BNC	WHT
B	- CLEAR	X	BNC	ORG
C	SER. CLOCK		J3 - E BNC	GRY
D				
E				
F	EOR	X	J5 - 16 BNC	YEL
H				
J				
K	- FLAG	X	J5 - 17 BNC	GRN
L				
M	BYTE COUNT 1	X	J5 - 3	ORG R
N	BYTE COUNT 0	X	J5 - 2	RED R
P				
R	ERROR	X	J5 - 1 BNC	BRN R
S				
T				
U				
V				
W				
X				
Y				
Z	GND		GND	BLK

Figure 11

BNC = FRONT PANEL BNC
R = RIBBON CABLE

J5 - BACK PANEL (TO COMPUTER)

PIN NO.	FUNCTION	SOURCE	CONNECTS WITH	COLOR
1	ERROR /COMP BIT 0		J4 - R BNC	BRN R
2	BYTE 0 /COMP BIT 1		J4 - N	RED R
3	BYTE 1 /COMP BIT 2		J4 - M	ORG R
4	DATA BIT 0/COMP BIT 3		J4 - 13	GRN R
5	DATA BIT 1/COMP BIT 4		J4 - 12	YEL R
6	DATA BIT 2/COMP BIT 5		J4 - 11	ORG R
7	DATA BIT 3/COMP BIT 6		J4 - 10	RED R
8	DATA BIT 4/COMP BIT 7		J4 - 9	BRN R
9	DATA BIT 5/COMP BIT 8		J4 - 8	BLK R
10	DATA BIT 6/COMP BIT 9		J4 - 7	WHT R
11	DATA BIT 7/COMP BIT 10		J4 - 6	GRY R
12	DATA BIT 8/COMP BIT 11		J4 - 5	VIO R
13	DATA BIT 9/COMP BIT 12		J4 - 4	BLU R
14	DATA BIT 10/COMP BIT 13		J4 - 3	GRN R
15	DATA BIT 11/COMP BIT 14		J4 - 2	YEL R
16	EOR		J4 - F BNC	YEL
17	- FLAG		J4 - K BNC	GRN
18				
19	GND		J5 - 20	BLK
20	GND		GND	BLK
21				
22				
23				
24				
25				
26				
27				
28				
29				
30				
31				
32				
33				
34				
35				
36				
37				

Figure 12

BNC = FRONT PANEL BNC
R = RIBBON CABLE

INTERFACE TO COMPUTER CONNECTIONS

COMPUTER I/O CARD PIN NO.	COMPUTER INPUT SIGNAL	INTERFACE OUTPUT SIGNAL	J5 PIN NO.	J4 PIN NO.
1	BIT 0	ERROR	1	12
2	BIT 1	BYTE 0	2	N
3	BIT 2	BYTE 1	3	M
4	BIT 3	DATA BIT 0	4	13
5	BIT 4	DATA BIT 1	5	12
6	BIT 5	DATA BIT 2	6	11
7	BIT 6	DATA BIT 3	7	10
8	BIT 7	DATA BIT 4	8	9
9	BIT 8	DATA BIT 5	9	8
10	BIT 9	DATA BIT 6	10	7
11	BIT 10	DATA BIT 7	11	6
12	BIT 11	DATA BIT 8	12	5
13	BIT 12	DATA BIT 9	13	4
14	BIT 13	DATA BIT 10	14	3
15	BIT 14	DATA BIT 11	15	2
16	BIT 15	EOR	16	F
23,AA	DEVICE FLAG	DEVICE FLAG	17	K
24,BB	GROUND	GROUND	19,20	Z

Figure 13

ACKNOWLEDGEMENTS

This work was supported by the Office of Naval Research under Contract N00014-76-C-0197, NR 083-400.

I would like to thank James McCullough and Albert J. Williams 3rd for their technical advice and encouragement, K. Pires and A. Henry for the typing, and S. Witzell for the graphics.

I would also like to thank the Memodyne Corporation for their permission to quote from their literature.

REFERENCES

Hewlett-Packard Co. (1972)

Operating and Service Manual: 12566B, 12566B-001, 12566-002 Microcircuit Interface Kits, Part #12566-90015 Hewlett Packard Co., 11000 Wolfe Road, Cupertino, CA 95014

Hunt, Mary (1976)

CARP, Cassette Reader Program, Vers. 17, W.H.O.I., Unpublished Manuscript

Memodyne Corp (a)

Cassette Recording for off-line Storage, Memodyne Corp., 385 Elliot Street, Newton Upper Falls, MA 02164

Memodyne Corp (b)

Instruction Manual, Model 3722, Memodyne Corp., 385 Elliot Street, Newton Upper Falls, MA 02164

Peal, K.R. (1973)

850 Current Meter - H.P. Interface, W.H.O.I., Unpublished Manuscript

Sams, H.W., Inc. (1975)

Reference Data for Radio Engineers, p. 40-22, Howard W. Sams and Co., Inc., New York, N.Y.

MANDATORY DISTRIBUTION LIST

FOR UNCLASSIFIED TECHNICAL REPORTS, REPRINTS, AND FINAL REPORTS
PUBLISHED BY OCEANOGRAPHIC CONTRACTORS
OF THE OCEAN SCIENCE AND TECHNOLOGY DIVISION
OF THE OFFICE OF NAVAL RESEARCH

(REVISED NOVEMBER 1978)

1 Deputy Under Secretary of Defense
(Research and Advanced Technology)
Military Assistant for Environmental Science
Room 3D129
Washington, D.C. 20301

Office of Naval Research
800 North Quincy Street
Arlington, VA 22217
3 ATTN: Code 483
1 ATTN: Code 460
2 ATTN: 102B

1 CDR J. C. Harlett, (USN)
ONR Representative
Woods Hole Oceanographic Inst.
Woods Hole, MA 02543

Commanding Officer
Naval Research Laboratory
Washington, D.C. 20375
6 ATTN: Library, Code 2627

12 Defense Documentation Center
Cameron Station
Alexandria, VA 22314
ATTN: DCA

Commander
Naval Oceanographic Office
NSTL Station
Bay St. Louis, MS 39522
1 ATTN: Code 8100
1 ATTN: Code 6000
1 ATTN: Code 3300

1 NODC/NOAA
Code D781
Wisconsin Avenue, N.W.
Washington, D.C. 20235

Woods Hole Oceanographic Institution
WHOI-79-75

A MEMODYNE 3722 CASSETTE READER SYSTEM FOR THE HP 2100 COMPUTER AND PROGRAM CARP by W. E. Terry. October 1979. 24 pages. Prepared for the Office of Naval Research under Contract N00014-76-C-0197; NR 083-400.

This report describes a special purpose electronic interface between the Memodyne 3722 High Speed Cassette Tape Reader and the Hewlett Packard 2100 series computer with program CARP using an HP 12566 interface. A description of the operation and alignment procedures is included.

1. Memodyne 3722 cassette
2. Cassette reader
3. CARP

I. Terry, W. E.
II. N00014-76-C-0197; NR 083-400

This card is UNCLASSIFIED

Woods Hole Oceanographic Institution
WHOI-79-75

A MEMODYNE 3722 CASSETTE READER SYSTEM FOR THE HP 2100 COMPUTER AND PROGRAM CARP by W. E. Terry. October 1979. 24 pages. Prepared for the Office of Naval Research under Contract N00014-76-C-0197; NR 083-400.

This report describes a special purpose electronic interface between the Memodyne 3722 High Speed Cassette Tape Reader and the Hewlett Packard 2100 series computer with program CARP using an HP 12566 interface. A description of the operation and alignment procedures is included.

1. Memodyne 3722 cassette
2. Cassette reader
3. CARP

I. Terry, W. E.
II. N00014-76-C-0197; NR 083-400

This card is UNCLASSIFIED

Woods Hole Oceanographic Institution
WHOI-79-75

A MEMODYNE 3722 CASSETTE READER SYSTEM FOR THE HP 2100 COMPUTER AND PROGRAM CARP by W. E. Terry. October 1979. 24 pages. Prepared for the Office of Naval Research under Contract N00014-76-C-0197; NR 083-400.

This report describes a special purpose electronic interface between the Memodyne 3722 High Speed Cassette Tape Reader and the Hewlett Packard 2100 series computer with program CARP using an HP 12566 interface. A description of the operation and alignment procedures is included.

1. Memodyne 3722 cassette
2. Cassette reader
3. CARP

I. Terry, W. E.
II. N00014-76-C-0197; NR 083-400

This card is UNCLASSIFIED

Woods Hole Oceanographic Institution
WHOI-79-75

A MEMODYNE 3722 CASSETTE READER SYSTEM FOR THE HP 2100 COMPUTER AND PROGRAM CARP by W. E. Terry. October 1979. 24 pages. Prepared for the Office of Naval Research under Contract N00014-76-C-0197; NR 083-400.

This report describes a special purpose electronic interface between the Memodyne 3722 High Speed Cassette Tape Reader and the Hewlett Packard 2100 series computer with program CARP using an HP 12566 interface. A description of the operation and alignment procedures is included.

1. Memodyne 3722 cassette
2. Cassette reader
3. CARP

I. Terry, W. E.
II. N00014-76-C-0197; NR 083-400

This card is UNCLASSIFIED

	BLK

BNC = FRONT PANEL BNC
R = RIBBON CABLE